UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

MLC INTELLECTUAL PROPERTY, LLC, Plaintiff, v. MICRON TECHNOLOGY, INC., Defendant.	Case No. 14-cv-03657-SI **SUPPLEMENTAL CLAIM CONSTRUCTION ORDER** Re: Dkt. Nos. 190, 191

On September 13, 2018, the Court held a hearing on defendant's request for supplemental claim construction. After consideration of the parties' arguments and the record, the Court issues this supplemental claim construction order.

BACKGROUND

On August 12, 2014, plaintiff MLC Intellectual Property, LLC ("MLC") brought suit against defendant Micron Technology, Inc., ("Micron") alleging infringement of United States Patent No. 5,764,571 ("the '571 Patent"). Dkt. No. 1. The '571 Patent is entitled "Electrically Alterable Non-Volatile Memory with n-bits Per Cell." The '571 Patent discloses non-volatile memory devices and methods of programming and/or verifying the programming of multi-level non-volatile memory devices. Non-volatile memory is capable of retaining the data with which it is programmed after the device is powered off. *See* '571 Patent 1:19-18; Dkt. No. 72-2 at ¶ 16. The memory device, made up of multiple semiconductor cells, has K^n predetermined memory states, where K is a base of a predetermined number system (such as 2 in the binary system of "1"

or "0"), n is the number of bits that can be stored in each cell,[1] and $K^n > 2$. '571 Patent at abstract.

On February 2, 2015, this case was stayed pending the resolution of IPR2015-00504 and IPR2-15-00571, which challenged the validity of the '571 Patent. Dkt. No. 31. The Patent Trial and Appeal Board ("PTAB") declined to institute an *inter partes* review ("IPR") of the '571 Patent, and this Court lifted the stay on March 29, 2016. Dkt. No. 43. On November 4, 2016, the Court entered a Claim Construction Order that construed terms 1 through 16[2] of the '571 Patent. Dkt. No. 95.

On July 31, 2017, Micron filed a request for *ex parte* reexamination with the United States Patent and Trademark Office ("USPTO") regarding the asserted claims of the '571 Patent. *See* Dkt. No. 170 at 7. On September 27, 2017, Micron gave notice that the PTAB granted its *ex parte* reexamination request. Dkt. No. 169. The Court again stayed this litigation, pending resolution of the reexamination. Dkt. Nos. 169, 176. In a non-final office action, the PTO found that claims 1, 9, 12, 30, 42, and 45 were rejected as unpatentable over Kitamura in view of Connolly.[3] Dkt. No. 190-3 at 5. MLC submitted Response A and Request for Continued Reexamination to overcome the non-final rejection.[4] Dkt. No. 190-4. MLC successfully overcame the non-final rejection, and

[1] Conventional memory cell devices allowed only two memory storage states in each cell based on the one bit of information the cell was capable of storing. '571 Patent at 1:24-26. Memory storage devices that were enhanced to allow multiple bits of storage per cell were either non-alterable read-only-memory systems or volatile memory devices not capable of permanent storage. *Id*. at 1:40-2:22. The '571 Patent attempts to solve this drawback by creating a "multi-level electrically alterable non-volatile memory (EANVM) device, wherein some or all of the storage locations have more than two states." *Id*. at 2:50-54.

[2] The parties adopted a numbering system for the terms at issue in their initial briefings that the Court adopted in its initial Claim Construction Order. Dkt. No. 95 at 6: 27-28. In the interest of consistency, the Court again adopts the parties' number system.

[3] The Board found in its preliminary assessment that Kitamura disclosed the elements of claim 1 of the '571 Patent with the exception of a "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information." Dkt. 190-3 at 6-8. This element was disclosed only when combined with Connolly which taught a double D/A converter wherein each converter had a resistor ladder. *Id.* at 7.

[4] Micron overcame the non-final rejection of all challenged claims by showing that between Connolly and Kitamura there was no teaching of "selection," no teaching of "a plurality of reference voltages," and no teaching of "reference voltages" that each "correspond to a different pre-determined memory state." *See generally*, Dkt. No. 190-4.

on June 28, 2018, the Examiner issued a Notice of Intent to Issue an *Ex Parte* Reexamination Certificate, indicating that the Examiner agreed with MLC's arguments and the patent claims were valid. Dkt. No. 180.

Micron now seeks supplemental claim construction of what it characterizes as a "new term" and terms 1, 2, 3, and 4 in light of statements that MLC made in Response A and Request for Continued Reexamination.

REQUESTED MODIFICATIONS

I. New Terms: "reference voltage(s)/reference signal(s)"

The terms "reference voltage(s)" and "reference signal(s)" were not previously construed as stand-alone terms. Construction of these terms would impact terms 1,[5] 5,[6] and 6[7] which have already been construed by the Court. Dkt. No. 95 at 25-28. Micron now asks the Court to construe these terms as "voltage(s) or signal(s) having a precise, known value that is/are constant over time." Dkt. No. 190 at 3:20-22. The term "reference voltage(s)" impacts the meaning of claim 1. The term "reference signal(s)" impacts the meaning of independent claims 3, 6, 9, 12, 15, 18, 21, 24, 27, 30, 33, 36, 39, 42, and 45. Claims 1 and 3 are representative claims that contain the terms at issue.

> 1. A multi-level memory device comprising:
>
> an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$;
>
> memory cell programming means for programming said multi-level memory cell in accordance with said input information;

[5] Term 1 is "selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed" and is used in claims 42 and 45.

[6] Term 5 is "reference voltage(s) . . . each of said reference voltages corresponding to a different one of said predetermined memory states" and is used in claim 1.

[7] Term 6 is "reference signal(s) . . . each reference signal corresponding to a different memory state of said memory cell" and is used in claims 9, 12, 30, 42, and 45.

reference voltage selecting means for selecting one of a plurality of **reference voltages** in accordance with said input information, each of said **reference voltages** corresponding to a different one of said predetermined memory states; and

comparator means for comparing a voltage of said multi-level memory cell with the selected **reference voltage**, said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information.

'571 Patent at 12:6-26 (emphasis added).

3. Multi-level memory apparatus, comprising:

an electrically alterable non-volatile memory cell having more than two predetermined memory states;

a selecting device which selects one of a plurality of **reference signals** in accordance with information indicating a memory state to which said memory cell is to be programmed, each **reference signal** corresponding to a different memory state of said memory cell; and

a comparator which compares a signal corresponding to the state of said memory cell with the selected **reference signal** to verify whether said memory cell is programmed to the state indicated by said information.

'571 Patent at 12:31-43 (emphasis added).

II. Term 1: "selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is programmed"

Term 1 is "selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed." Dkt. No. 95 at 25:8-9. This term was previously construed by the Court to mean "selecting one of a plurality of reference signals that corresponds to a memory state to which the memory cell is to be programmed." *Id.* at 27:3-6. Micron now asks the Court to reconstrue this term as "selecting one from amongst at least four pre-determined ~~of a plurality~~ reference signals that corresponds to a memory state to which the memory cell is to be programmed, where selecting is performed without converting input information to an output voltage and is performed without use of a circuit to output a voltage from a resistor ladder."[8] Dkt. No.190 at 4:6-10. This term impacts the meaning of claims 42 and 45. Below is a representative claim that contains the term at issue.

[8] Unless otherwise noted, Micron asks the Court to add the underlined phrases and remove the struck phrases from each term's construction.

> 45. A method of programming an electrically alterable non-volatile memory cell having more than two predetermined memory states, said method comprising:
>
> **selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed,** each reference signal corresponding to a different memory state of said memory cell;
>
> applying a programming signal to said memory cell; and controlling the application of said programming signal to said memory cell based on the selected reference signal.

'571 Patent at 16:42- 49 (emphasis added).

III. Terms 2 and 3: "selecting device which selects one of a plurality of [predetermined] reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed"

Terms 2 and 3 are very similar and were construed together as one term by the Court in the Claim Construction Order. Together, the term is "selecting device which selects one of a plurality of [predetermined][9] reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed." Dkt. No. 95 at 14:15-17. The Court found that the term "selecting device" was a generic term and construed it as means-plus-function term. Dkt. No. 95 at 16:2-18. The structure is a "verify reference select circuit, pictured as example only in Fig. 8 as item 222,"[10] with the function of "selecting one of a plurality of [predetermined] reference signals that corresponds to a memory state to which the memory cell is to be programmed." Dkt. No. 95 at 16:18-23. Micron now asks the Court to reconstrue the collective term as having a function of "selecting one from amongst at least four pre-determined ~~of a plurality of [predetermined]~~ reference signals that corresponds to a memory state to which the memory cell is to be programmed, where selecting is performed without converting input information to an output voltage." Micron also seeks to reconstrue the structure as a "verify reference select circuit, excluding a circuit that outputs a voltage from a resistor ladder." *Id.*

[9] The word "predetermined" is included in claim 9 but not included in claims 12 or 30. The language is otherwise the same. For this reason, terms 2 and 3 which, are taken from claim 9 and from claims 12 and 30 respectively, were construed together.

[10] The parties agreed at the hearing that all terms construed under § 112(f) include equivalent structures, and not "engineering equivalents." Dkt. No. 95 at 8:27-28.

Term 2 impacts the meaning of claim 9. Term 3 impacts the meaning of claim 12, and 30. Below is a representative claim that contains the term at issue.

> 9. Multi-level memory apparatus, comprising:
>
> an electrically alterable non-volatile memory cell having more than two predetermined memory states;
>
> **a selecting device which selects one of a plurality of predetermined reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed**, each reference signal corresponding to a different memory state of said memory cell;
>
> a programming signal source which applies a programming signal to said memory cell; and
>
> a comparator which compares a signal corresponding to the state of said memory cell with the selected reference signal to verify whether said memory cell is programmed to the state indicated by said information.

'571 Patent at 13: 1-14 (emphasis added).

IV. Term 4: "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information"

Term 4 is a "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information." Dkt. No. 95 6:17-18. This term was previously construed by the Court as a means-plus-function term. The function is "selecting one of a plurality of reference voltages in accordance with the input information" with a corresponding structure of a "verify reference select circuit." *Id.* at 8:23-25. Micron now asks the Court to reconstrue this term so that the function is "selecting one from amongst at least four pre-determined ~~of a plurality of~~ reference voltages in accordance with the input information, where selecting is performed without converting input information to an output voltage." Micron also asks the court to reconstrue the structure as a "verify reference select circuit, excluding a circuit that outputs a voltage from a resistor ladder." This term impacts the meaning of claim 1.

> 1. A multi-level memory device comprising:
>
> an electrically alterable non-volatile multi-level memory cell for storing input information in a corresponding one of K^n predetermined memory states of said multi-level memory cell, where K is a base of a predetermined number system, n is a number of bits stored per cell, and $K^n > 2$;

memory cell programming means for programming said multi-level memory cell in accordance with said input information;

reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information, each of said reference voltages corresponding to a different one of said predetermined memory states; and

comparator means for comparing a voltage of said multi-level memory cell with the selected reference voltage, said comparator means further generating a control signal indicating whether the state of said multi-level memory cell is the state corresponding to said input information.

'571 Patent at 12:6-26 (emphasis added).

LEGAL STANDARD

Claim construction is a matter of law. *Markman v. Westview Instr., Inc.*, 517 U.S. 370, 372 (1966). Terms contained in claims are "generally given their ordinary and customary meaning." *Phillips v. AHW Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). In determining the proper construction of a claim, a court begins with the intrinsic evidence of record, consisting of the claim language, the patent specification, and, if in evidence, the prosecution history. *Id*. at 1313. Claim terms are construed in light of their ordinary and accustomed meaning, unless examination of the specification, prosecution history, and other claims indicates that the inventor intended otherwise. *See Electro Medical Sys., S.A. v. Copper Life Sci., Inc.*, 34 F.3d 1048, 1053 (Fed. Cir. 1994).

The prosecution history limits the interpretation of the claim terms so as to exclude any interpretation that was disclaimed during prosecution. *See Southwall Tech., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995). "A patentee's statements during reexamination can be considered during claim construction, in keeping with the doctrine of prosecution disclaimer." *Krippelz v. Ford Motor Co.*, 667 F.3d 1261, 1266 (Fed. Cir. 2012). Considering these statements "will ensure that claims are not argued one way in order to maintain their patentability and in a different way against accused infringers." *Aylus Networks, Inc. v. Apple Inc.*, 856 F.3d 1353, 1360 (Fed. Cir. 2017) (applying the doctrine of prosecution disclaimer to statements before the PTAB during IPR proceedings).

However, prosecution history "often produces ambiguities created by ongoing negotiations between the inventor and the PTO." *Grober v. Mako Prods., Inc.*, 686 F.3d 1335, 1342 (Fed. Cir. 2012) (citing *Abbot Labs v. Sandoz, Inc.*, 566 F.3d 1282, 1289 (Fed. Cir. 2009)). As a result, "the doctrine of prosecution disclaimer only applies to unambiguous disavowals." *Id.* The patentee must make statements of "manifest exclusion or restriction, representing a clear disavowal of claim scope." *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1324 (Fed. Cir. 2002).

DISCUSSION

Micron asks the Court to narrow previously construed terms of the '571 Patent in light of MLC's statements during the *ex parte* reexamination. MLC contends that the reexamination did not change the file history and that it did not make any statements that limit claim scope. MLC therefore asserts that Micron waived its ability to bring new arguments because they should have been made at the first claim construction hearing. This Court must consider whether Micron waived its arguments, and whether there are file history changes that amount to clear disavowals of claim scope.

I. Waiver

MLC asks the Court to deny Micron's requested claim construction modifications. MLC argues that Micron has waived all of its current arguments by not raising them during the initial claim construction. MLC contends that it had the same responses to the *ex parte* reexamination as it did to the IPR in which defendant asserted the same prior art and arguments against the '571 Patent and, as a result, the '571 Patent's file history is unchanged. Dkt. No. 191 at 1.

Generally, litigants waive claim construction disputes if they fail to raise them before trial. *See Lazare Kaplan Int'l, Inc. v. Photoscribe Techs., Inc.*, 628 F.3d 1359, 1376 (Fed. Cir. 2010); *Broadcom Corp. v. Qualcomm Inc.*, 543 F.3d 683, 694 (Fed. Cir. 2008) (finding a waiver where parties argued for construction in post-trial motions). However, claim construction disputes that arise before trial are not waived when both parties and the court are aware of the dispute. *See, e.g., GPNE Corp. v. Apple Inc.*, 830 F.3d 1365, 1372 (Fed. Cir. 2016).

"The ultimate question of construction [is] a legal question," which "is for the judge and not the jury." *Teva Pharm. USA, Inc., v. Sandoz, Inc.*, 135 S.Ct. 831, 841 (2015). "When the parties present a fundamental dispute regarding the scope of a claim term, it is the court's duty to resolve it." *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008). If a "fundamental dispute"[11] about the scope of a claim arises after claim construction but before trial, the court is obliged to clarify the term. *Altera Corp. v. PACT XPP Techs. AG*, No. 14-cv-02868-JD, 2015 WL 4999952, at *8 (N.D. Cal. Aug. 21, 2015) (requiring claim construction after expert discovery and motion practice revealed a fundamental dispute after the court had construed the claims).

To the extent that the file history changed as a result of the *ex parte* reexamination and there is an actual dispute between the parties, the Court must reconsider claim construction. The Court will not, however, reconstrue terms for which the file history has not changed because those disputes have already been addressed.

II. Changes to File History

A patent is limited by its file history when the patentee makes statements of "manifest exclusion or restriction, representing a clear disavowal of claim scope." *Teleflex*, 299 F.3d at 1325. However, "applicants rarely submit affirmative disclaimers along the lines of 'I hereby disclaim the following . . .' during prosecution and need not do so to meet the applicable standard." *Saffran v. Johnson & Johnson*, 712 F.3d 549, 559 (Fed. Cir. 2013). "When the alleged disclaimer is ambiguous or amenable to multiple reasonable interpretations, [the court] decline[s] to find prosecution disclaimer." *Core Wireless Licensing S.A.R.L. v. LG Elecs., Inc.*, 880 F.3d

[11] The courts have not clearly defined what constitutes a fundamental dispute. *See Novelbiz, Inc. v. Global Connect, L.L.C.*, 876 F.3d 1326, 1328 (Fed. Cir. 2017) (O'Malley, C.J., dissenting) (dissenting from the denial of a petition for rehearing en banc to resolve when an "actual dispute" exists for claim construction). While district courts "are not (and should not be) required to construe every limitation," the Court must construe disputed terms that govern the technical scope of a claim. *O2 Micro*, 521 F.3d at 1362. *See, e.g., Biotec Biologische Naturverpackungen GmbH & Co. KG v. Biocorp, Inc.*, 249 F.3d 1341, 1349 (Fed. Cir. 2001); *U.S. Surgical Corp. v. Ethicon, Inc.*, 103 F.3d 1554, 1568 (Fed. Cir. 1997).

1356, 1367 (Fed. Cir. 2018) (citing *Mass. Inst. of Tech. v. Shire Pharm., Inc.*, 839 F.3d 1111, 1119 (Fed. Cir. 2016)).[12]

The Court considers each of the alleged changes to the file history of the '571 Patent and will then determine whether any changes amount to clear disavowals of claim scope.

A. New Terms: "Reference Voltage(s)/Signal(s)"

Micron clarified at oral argument that it is asking for "reference voltage(s)" and "reference signal(s)" to be construed as two separate terms that have the same limitations, rather than one term in which voltages and signals are synonymous. The Court agrees that the two terms should not be collapsed into one definition. During the argument, Micron asked the Court to find that the term "reference" has specialized meaning in the art and should be applied to voltages and signals in the same way throughout the patent. Micron argued that MLC made disclaimers that were directed at the word "reference," not the term "reference voltage." However, during the reexamination, MLC provided a technical definition for "reference voltage." Dkt. No. 190-4 at 7. The Court finds that this statement was directed to "reference voltage(s)" as a term of art and declines to consider "reference" as a stand-alone term.

1. Reference Voltage

Micron asks the Court to construe the term "reference voltage(s)" as "voltage(s) . . . having a precise, known value that is/are consistent over time." Dkt. No. 190 at 5:2-4. The Court

[12] At oral argument Micron urged the Court to reconstrue claims based on statements that MLC made during the reexamination which did not constitute clear and unambiguous disavowals because "any statement made . . . during prosecution is given weight, serves the public notice function, and may be considered to constitute a disclaimer." *See Implicit L.L.C. v. F5 Networks, Inc.*, No. 14-CV-02856-SI, 2015 WL 2194626, at *14 (citing *Elkay Mfg. Co. v. Ebco. Mfg. Co.*, 192 F.3d 973, 979 (Fed. Cir. 1999). In *Implicit*, this Court held that a patentee's argument to the PTAB constituted disavowal even though the examiner did not accept that argument. Similarly, in *Elkay Mfg. Co. v. Ebco. Mfg. Co.*, the court held that when the patentee makes an argument that "necessarily relinquishe[s] a construction of [the patent's] claim language[,]" the argument is "given the same weight as claim amendments." 192 F.3d 973, 979 (Fed. Cir. 1999). While the Court considers every statement and every statement may be considered to constitute a disclaimer, it is only arguments to the PTAB that necessitate a disclaimer of claim scope. The Court declines to find prosecution disclaimer when a statement is ambiguous or amenable to multiple reasonable interpretations. *See Core Wireless*, 880 F.3d at 1367.

construed the phrase "reference voltage(s)" part of term 5[13] in the Claim Construction Order. Dkt. No. 95, 25-28. At that hearing, the Court declined to construe "reference voltage(s)" as "voltage value(s)" because such a construction would confuse claim 1 and claim 2.[14] *Id.* at 27:24-27. The Court relied on MLC's Claim Construction Brief to reach this construction. MLC's brief proposed "adopt[ing] the plain and ordinary meaning of 'reference voltage(s)' and recogniz[ing] that the person of ordinary skill in the art would understand that 'reference voltage(s)' are distinct voltage(s) that correspond to a particular memory state." Dkt. No. 72 at 7:1-3.

During the *ex parte* reexamination MLC advocated that "[t]he term 'reference voltage' has a specific meaning in the art." Dkt. No. 190-4 at 7. MLC used the Institute of Electrical and Electronics Engineers (IEEE) Standard Dictionary to confirm that "reference voltage(s)" is a "[a] separate, highly regulated voltage source used as a standard to which the output of the power supply is continuously referred." *Id*. After establishing that "reference voltage(s)" has a "specific meaning" rather than its plain and ordinary meaning, MLC used this "specific meaning" to distinguish the '571 patent from two prior art references. MLC argued in the reexamination that, as a result, the voltages disclosed in prior art were not reference voltages because they were "not as precise or stable as required of the voltages from the '571 patent." *Id*. The Court finds that MLC's representation changes the file history.

The Court agrees with defendant that plaintiff's use of a specialized definition to characterize "reference voltage" and distinguish the patent amounts to a clear and unmistakable disclaimer. Because "reference voltage(s)" must meet this specific standard, the Court adopts Micron's proposed language and holds that the term "reference voltage(s)" is construed as "voltage(s) having a precise, known value that is/are constant over time." This new construction of "reference voltage(s)" impacts the meaning of claim 1.

Micron also asks the Court to restrict the '571 Patent's use of resistor ladders because

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[13] Term 5 is "reference voltage(s) . . . each of said reference voltages corresponding to a different one of said predetermined memory states."

[14] "Voltage values" were specifically claimed in Claim 2 of the '571 Patent. '571 Patent at 12:27-30. The Court declined to construe "reference voltage" as "voltage value" because doing so would confuse the distinct claims. Dkt. No. 95 at 27:24-27.

MLC stated that that voltages "converted into other voltages . . . through the use of resistors and buffers" are not reference voltages and that that voltages produced from a resistor ladder "cannot correspond to any pre-determined memory state." *Id.* at 7:23-25 (citing Dkt. No. 190-4 at 8); 8:17-20 (citing Dkt. No. 190-4 at 11). Because these statements relate more to the qualities of reference voltages than to the use of a resistor ladder, they are addressed here. The new construction of "reference voltage(s)" requires that the voltage be sufficiently precise. The new construction precludes imprecise voltages, like those that have been converted through a resistor ladder, from being reference voltages. Similarly, claim 1 already requires that "reference voltages correspond[] to a different one of said predetermined memory states." '571 Patent at 12:18-20. Therefore, when read in context of the claim, the new construction is consistent with MLC's statements.

2. Reference Signal

Micron asks the Court to limit the term "reference signal(s)" to "signal(s) having a precise, known value that is/are constant over time." Micron contends that MLC used the terms "reference signal(s)" and "reference voltage(s)" interchangeably during the reexamination and, therefore, the same limiting definition should apply to signal(s) and voltage(s). Dkt. No. 190 at 5:24-27. Micron relies on MLC's statement in the reexamination in which MLC argued, "The claims, as well as the Specification of the '571 patent, repeatedly and explicitly require that the 'reference voltages' or 'reference signals' correspond to a pre-determined memory state." Dkt No. 190 at 5:24-28; Dkt. No. 190-4 at 9-10. This is the sole instance where reference signals and reference voltages are discussed together during the reexamination.

The Court's current construction of term 1[15] already requires that reference signals "correspond to a memory state to which the memory cell is to be programed." Dkt. No. 95 27:3-6. Similarly, the construction of term 6[16] requires that each reference signal "corresponds to a

[15] Term 1 is "selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed."

[16] Term 6 is "reference signal(s) . . . each reference signal corresponding to a different

different memory state of the memory cell." *Id*. at 28:26-28. The Court declined to construe "reference signal(s)" as an "analog verify signal value(s)" because, as Micron's expert Michael Headley admitted, "signal" is a broader term than "voltage." *Id*. at 28:11-14. MLC's expert, Jack Lee, testified that the terms signal and voltage "are not interchangeable and have distinct well-known meanings within the field of circuitry and memory devices." Dkt. No. 76-6, ¶ 4. MLC's single statement that both voltages and signals are required to correspond to a pre-determined memory state does not overcome the extensive file history that shows that the two terms are not interchangeable. This statement is insufficient to show that the file history changed.

B. Voltage Conversion and Resistor Ladders

1. "Selecting . . . Reference Signals in Accordance with Information Indicating a Memory State"

Micron seeks to modify the selection process of terms 1 through 4[17] with the limitation "where selecting is performed without converting input information to an output voltage." Dkt. No. 190 at 7:2-6. Micron concedes that MLC distinguished "selection" from "conversion" in the IPR. Dkt. No. 190 at 7:12-14. During the IPR, MLC overcame prior art by arguing that a digital-to-analog conversion circuit failed to make a selection of any kind, "let alone a selection of a plurality of reference voltages." *Id*; *see also,* Dkt. No. 34-1 at 10-11, 15. Based on these representations, this Court adopted the plain and ordinary meaning of term 4, "selecting one of a plurality of reference voltages in accordance with input information," with the corresponding structure of a verify reference select circuit.[18] Dkt. No. 95 at 6-8.

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memory state of said memory cell."

[17] Each of these terms describes selecting one of a plurality of reference signals in accordance with memory or input information. Term 1 is "selecting one of a plurality of reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed." Terms 2-3 are "selecting device which selects one of a plurality of [predetermined] reference signals in accordance with information indicating a memory state to which said memory cell is to be programmed." Term 4 is "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information."

[18] In the initial Claim Construction Order, the Court agreed with Micron that a "selection circuit" could not be a corresponding structure because the specification does not specifically disclose and tie that structure to the disclosed function. Dkt. No. 95 at 7:17-8:2. Instead, the

In the reexamination, MLC again overcame prior art by asserting that "the prior art references cannot select from amongst a *plurality* of reference voltages because they only have a *single* reference voltage." Dkt. No. 190-4 at 7 (emphasis in original). MLC's representation of the difference between selection and conversion is substantially the same in the IPR and in the reexamination proceedings. MLC has consistently asserted that conversion of a single reference voltage is not a selection because only one reference voltage was available to convert. MLC did not distinguish its invention from prior art on the basis that the invention did not convert input information to an output voltage. *Id.* Instead, MLC distinguished its invention by asserting that there must be a selection from a plurality of inputs. *Id.*; *see also*, Dkt. No. 190-8 at 6-8. Therefore, there has not been a change to the file history with respect to this limitation of terms 1 through 4.

Furthermore, Micron asked the Court in its original Claim Construction Brief to limit these terms to a device "having as its output an analog voltage reference signal." Dkt. No. 75 at 8:19-23, 11:10-12. Micron's initial proposed construction clearly indicates that the patented invention can convert an input signal to an output voltage as a part of the selection process. This Court rejected that limitation because "there is nothing about the function 'selecting one of a plurality of reference voltages in accordance with the input information' that requires 'having as its output an analog voltage reference signal.'" Dkt. No. 95 at 8:6-8. However, Micron, MLC, and the Court understood that conversion may be a part of selection based on the intrinsic record. It does not follow that because conversion is not selection that all selection methods must exclude conversion. The Court will not consider Micron's new position that conversion must be entirely excluded from selection.

2. Resistor Ladder

Micron asks the Court to reconstrue terms 1 through 4 to exclude structures that use

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specification clearly linked the verify reference select circuit to the function recited in the claim. *See* '571 Patent at 8:34-43; 8:66-9:7. This circuit is an element in the circuit displayed in Figure 8 but is not limited to this structure. Dkt. No. 95 at 8:23-9:2.

resistor ladders[19] based on statements made by MLC during the *ex parte* reexamination. Dkt. No. 190 at 7:23-25. Micron contends that MLC disclaimed the use of any resistor ladders by stating that voltages "converted into other voltages . . . through the use of resistors and buffers" are not reference voltages, that voltages produced from a resistor ladder "cannot correspond to any pre-determined memory state," and that the '571 Patent "completely remov[ed] resistor ladders/step-voltages." *Id.* at 7:23-25 (citing Dkt. No. 190-4 at 8); 8:17-20 (citing Dkt. No. 190-4 at 11); 8:24-25 (citing Dkt. No. 190-4 at 12). The first and second statements, which relate to whether a voltage from a resistor ladder can be a reference voltage or can correspond to a pre-determined memory state, are more applicable to the Court's construction of "reference voltage(s)." Both of these statements confirm that a reference voltage may require certain properties, including corresponding to a pre-determined memory state. However, these statements generally do not limit the invention to embodiments without resistor ladders and have been already been addressed *supra* II (A)(1).

In contrast, the third statement identified by Micron, that the '571 Patent completely removed the need for resistor ladders, warrants further consideration. To distinguish its invention from prior art, MLC wrote that "[t]he '571 patent overcame [an inconsistency] problem by, among other things, completely removing resistor ladders/step-voltages." Dkt. No. 190-4 at 12. Instead, the '571 Patent's invention selects "from amongst pre-defined reference voltage levels that each correspond to a different predetermined memory state." *Id.* Neither the patentee's responses to the PTAB during the IPR proceeding nor the patent specification mention the complete removal of resistor ladders/step-voltages. This new disclosure changes the file history.

MLC responds that it simply described features of Connolly to show that it was cumulative to VLSI and did not distinguish its invention on this basis. Dkt. No. 191 at 4 ("The prior art shown in Connolly is the exact same as that shown by VLSI . . . it contains a resistor ladder with a

[19] A resistor ladder is a chain of resistors used to achieve a variable output voltage. Dkt. No. 190-4 at 4. A resistor ladder takes one reference voltage as an input and passes it through a chain of resistors, all with a fixed proportion of resistance R. *Id*. The output voltage is determined by the resistors in the ladder and is "dependent upon characteristics and uncertainty inherent in the resistors." *Id.* at 8. This piece of electrical circuitry is not mentioned in the '571 Patent but was used in Connolly, asserted in the reexamination, and in VLSI, asserted in the IPR.

digital input switches and a single reference voltage."). MLC relies on *Grober v. Mako Products, Inc.* for the argument that prosecution disclaimer does not apply when the claimed invention is not distinguished from prior art on the basis of a particular feature but the feature is merely described. 686 F.3d 1335, 1342 (Fed. Cir. 2012) (finding no disclaimer where "the applicant simply describes features of the prior art and does not distinguish the claimed invention based on those features.")

The Court is not persuaded by MLC's argument. In the reexamination, MLC wrote that there were problems of imprecision in the prior art and "[t]he '571 Patent overcame this problem by, among other things, completely removing resistor ladders/step-voltages and, instead, selecting from amongst pre-defined reference voltage levels that each correspond to a different predetermined memory state." Dkt. No. 190-4 at 12. This statement goes beyond merely describing prior art and characterizes the present invention as one that excludes resistor ladders/step-voltages because such systems have "unknown output voltages" and are subject to "errors characteristics" and "inherent uncertainty." *Id.* The Federal Circuit has made clear that "an applicant's argument that a prior art reference is distinguishable on a particular ground can serve as a disclaimer of claim scope even if the applicant distinguishes the reference on other grounds as well." *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1374 (Fed. Cir. 2007).

MLC's representation that the '571 Patent's complete removal of resistor ladders distinguishes it from prior art constitutes unambiguous disavowal of claim scope. Accordingly, the Court reconstrues the structure of claims 1, 9, 12, and 30 (terms 2, 3, and 4) as a verify reference select circuit, excluding a circuit that outputs a voltage from a resistor ladder. Similarly, the Court reconstrues claims 42 and 45 (term 1) to include the phrase "where selecting is performed without use of a circuit to output a voltage from a resistor ladder." However, the Court notes that this new construction does not remove all circuits with resistor ladders from the scope of the invention. The construction requires that selection be made without the use of a resistor ladder in the verify reference select circuit, not that any circuit that has a reference select circuit be devoid of resistor ladders which may be included for non-selection purposes. For

example, a verify reference select circuit without a resistor ladder that is used in a larger circuit that has resistor ladders would be within the scope of the '571 Patent.

C. Selection from at Least Four Reference Voltages

Micron asks the Court to modify the construction of terms 1-4 to the extent that the terms require selecting one of a plurality of reference voltages. Dkt. No. 190 at 9:26-10:6. At the initial claim construction hearing, the parties initially disagreed over whether "plurality" should be defined as "a set," as requested by MLC, or be given its plain and ordinary meaning, as requested by Micron. Dkt. No. 95 at 6:19-28. The parties subsequently agreed that "plurality" was acceptable and no further construction was considered.[20] *Id.* Micron now argues that MLC's statement during the reexamination requires that "plurality" be construed to mean "at least four" and that MLC disclaimed systems with fewer than four reference voltages.

Micron argues that "logic mandates that there be at least four reference voltages" to "implement a memory cell with more than one logic level using the structures claimed by the '571 Patent." Dkt. No. 190 at 10. Micron's expert, McAlexander, opined that this circuit requires at least four memory states because each memory cell "must necessarily have 2^n memory states" where "n is a whole number greater than 1." Dkt. No. 190-2 at ¶ 47. However, this argument does not stem from any new information in the reexamination. The Court is not persuaded that "logic mandates" this construction because neither MLC nor Micron reached this conclusion at the initial claim construction.

Micron also bases its argument on two of MLC's statements during the *ex parte* reexamination. MLC stated that "the '571 patent describes the programming steps as requiring selecting amongst at least four pre-determined reference voltages based on the digital input." Dkt. No. 190-4 at 10:1-3. MLC further provided an example of selecting from among four predetermined voltages to show how the '571 Patent makes a selection. *Id*. at 11. MLC contends that this statement was "merely a description of how the programming . . . is implemented in a

[20] MLC agreed that "plurality" would be construed according to its plain and ordinary meaning during oral argument at the Claim Construction Hearing. *See* Dkt. No. 95 at 6:19-28.

specific embodiment of the '571 patent where a memory cell has four memory states." Dkt. No. 191 at 6. MLC further argues that this statement was made with respect to the PTAB's understanding of term 5 ("reference voltages corresponding to different memory states"), not term 4 ("a plurality of reference voltages"), and should be understood to refer to the scope of only term 5. *Id.*

The preferred embodiment of the '571 Patent and the majority of the descriptions in the specifications "assume a binary system which stores 2-bits per memory cell." '571 Patent 4:38-40. To illustrate this, the specification describes an embodiment where "n is set to 2 and one of four states of the memory cell must be detected." *Id.* at 7:12-14. The patent specification explicitly discloses "four possible states" of memory that can be detected, "(0,0), (0,1), (1,0), or (1,1)." *Id.* at 7:14-15. However, the scope of an invention is not limited to the scope of a preferred embodiment to the exclusion of other embodiments. *See Phillips*, 415 F.3d at 1313 (Fed. Cir. 2005) ("[A]lthough the specification often describes very specific embodiments of the invention, we have repeatedly warned against confining the claims to those embodiments."). Indeed, the '571 Patent expressly contemplates other non-binary systems. Specifically, the specification states:

> The concepts of the invention extend to systems where n is greater than 2. It is also intended that the invention include any system where the EANVM memory cell has more than two states. For example, in a non-binary system, the memory states can be three or some other multiple of a non-binary system.

'571 Patent at 8:11-16.

The example of four reference voltages from which the invention chooses and the underlying system logic were aspects of the invention long before MLC responded to the *ex parte* reexamination. Only MLC's statement that the '571 Patent has a "requirement" of selecting amongst four or more voltages is new. Given the strong language MLC used, the Court finds that this is a change to the file history.

Prosecution history must be read in context of the entire file history, rather than in isolation. *See Massachusetts Inst. of Tech. v. Shire Pharm., Inc.*, 839 F.3d 1111, 1120 (Fed. Cir. 2016) (quoting *Ecolab, Inc. v. FMC Corp.*, 569 F.3d 1335, 1342 (Fed. Cir. 2009) ("Even if an

isolated statement appears to disclaim subject matter, the prosecution history as a whole may demonstrate that the patentee committed no clear and unmistakable disclaimer.")). MLC contends that its statement does not disclaim claim scope because, when read in context, (1) it was limited to a specific embodiment and (2) was used to clarify how reference voltages correspond to memory states, rather than the number of reference voltages.[21] Dkt. No. 191 at 6.

1. Specific Embodiment

The vast majority of the '571 Patent's specification focuses on a preferred, binary embodiment of the invention. *See, e.g.*, '571 Patent at 4:21-30; 7:9-15; 8:9-11. When describing this embodiment, the specification refers multiple times to the detection and selection of four possible states or voltages. *Id.* at Fig. 7; 7:9-15; 7:55-57. For example, the specification states:

> FIG. 6 shows a binary system 150 for reading the state of an n-bit floating gate memory cell 102, as described in connection with FIG. 1, according to the invention, where n is the number of bits stored in the memory cell. For this example, n is set to 2 and one of four states of the memory cell must be detected. The four possible states being, (0,0), (0,1), (1,0), or (1,1).

'571 Patent at 7:8-15.

In its response to the *ex parte* reexamination, MLC stated that there had to be a selection from amongst pre-determined memory states. Dkt. No. 190-4 at 9-10. MLC specifically noted that the reference voltages "are chosen based on the characteristics of the memory cell" and "[t]he pre-determined memory state is therefore dependent on the characteristics of the cell." *Id.* These statements are limited by the "characteristics of the cell" and, therefore, do not apply to memory cells that have different characteristics. The specification notes that while "a binary 2-bit cell system is shown" the invention includes "systems where n is greater than 2." '571 Patent at 8:9-12. "For example, in a non-binary system, the memory states can be three or some other multiple of a non-binary system." *Id.* at 8:14-16.

Therefore, MLC's statement reasonably can be seen as applying only to binary memory

[21] Specifically, MLC argues that the statement at most limits term 5 and not term 4. Term 5 is "reference voltage(s) . . . each of said reference voltages corresponding to a different one of said predetermined memory states." Term 4 is "reference voltage selecting means for selecting one of a plurality of reference voltages in accordance with said input information."

systems with four memory states. Because this is a reasonable construction of MLC's statement that "requir[ed] selecting amongst at least four pre-determined reference voltages," the Court declines to construe "plurality" as "at least four." The Court maintains its previous construction and construes "plurality" to have its plain and ordinary meaning.

2. Modification of Term 5

MLC also contends that, in context, its statements should at most limit term 5 but not term 4. Dkt. No. 191 at 6. Because the Court has already found that MLC's statement did not unambiguously limit claim scope, the Court declines to consider this argument.

CONCLUSION

For the foregoing reasons and for good cause shown, the Court hereby adopts Microns proposed claim constructions with respect to limiting the term "voltage signal(s)" and the removal of resistor ladders from selection circuits. The Court maintains its previous constructions for all other terms and declines to adopt Micron's proposed modifications.

IT IS SO ORDERED.

Dated: September 26, 2018

SUSAN ILLSTON
United States District Judge

United States District Court
Northern District of California